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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER	
AGGARWAL, YOGESH K	
ART UNIT	**PAPER NUMBER**
2615	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/680,239	PAIN ET AL.	
	Examiner	Art Unit	
	Yogesh K. Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-6,12-15 and 18* is/are allowed.

6)☒ Claim(s) *1,2,7-11,16,17,19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed 04/07/2005 have been fully considered but they are not persuasive.

Examiner's response:

2. Applicant argues with regards to claim 1 (Amendment, pp 16 and 17) that "Zhou (US Patent # 6,787,749) discloses a sensor array for receiving input signals, a frame memory array for temporarily storing a full frame, and an array of self-calibration column integrators for uniform column-parallel signal summation (Zhou: Abstract). However, Claim 1 teaches an imaging device including a photo-sensing array and an integrator array ... wherein integrators of each column are coupled to receive electrical pixel signals in said photo-sensing array. Therefore, Zhou discloses that electrical pixel signals are stored in a frame memory array and the integrators receive the signals from the frame memory array (Zhou: Col. 2, lines 34-42; Fig. 1A; Col. 3, lines 33-62). In contrast, Claim 1 recites receiving signals from the photo-sensing array, and not from a frame memory array". The Examiner respectfully disagrees. As pointed out in the previous office action, the frame memory array 130 was being broadly read as an integrator array for the following reasons. It is very well known in the art to have a memory that is formed of capacitors that not only serve to integrate the photoelectric current at the same time, i.e., to convert it into a voltage signal, and to store this voltage signal. The voltage level is being dependent on the photoelectric current and proportional to the integration time and inversely proportional to the integration capacity i.e. $V=1/C\ (\int Idt)$. Therefore, as broadly as claimed, the frame memory array can serve both as a storage device and an integrator.

3. Applicant further argues with regards to claim 1 (Amendment, pp 17) that Zhou '749 fails to disclose an integrator array of a plurality of integrators arranged in rows and columns respectively equal to said N rows and columns of said photo-sensing array. The Examiner respectfully disagrees. As explained above, the Examiner is broadly reading the frame memory array as an integrator array, Zhou teaches that the frame memory 130 has memory cells with one-to-one correspondence with the active pixel cells of the APS array (col. 3 lines 43-45). Therefore an integrator array of a plurality of integrators arranged in rows and columns respectively equal to said N rows and columns of said photo-sensing array as recited in claim 1.

4. Applicant argues with regards to claim 16 (Amendment, pp 19) that although Antonelli (US Patent # 6,259,108) suggests using CMOS APS pixels, there is no suggestion or teaching in neither Antonelli '108 nor Hasegawa (US Patent # 5,917,620) on how to combine an active electrical pixel signal generated within the sensing array (not an accumulated charge transfer out of the sensing array) to "sample multiple frames of images of the object generated by the sensing array" by "coupling a linear array of integrators to the sensing array" as recited in Claim 16. The Examiner respectfully disagrees. Hasegawa '620 teaches a method comprising using a linear sensing array of pixels (col. 2 lines 65-67, figure 6, element 1701-1703) coupling a linear integrator array (1710, 1712) of integrators sensing array to sample object generated by multiple frames sensing array (col. 3 lines 12-21) and images of the spatially shifting the mapping from the sensing frames along the predetermined direction to produce a summed signal that sums pixel signals from different pixel locations different frames corresponding common image from a location on object (col. 2 lines 56-64). Antonelli '108 was merely used to show that a linear sensor array formed of CCDs as taught in Hasegawa may use CCD (charge coupled device)

pixels, or may use CMOS (complementary metal oxide semiconductor) APS (active pixel sensing) pixels, photo-diode pixels, or any other linear array of light sensing technology (col. 4 lines 17-24). Therefore taking the combined teachings of Hasegawa and Antonelli, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have an in-pixel circuit internally converting radiation-induced charge into an electrical pixel signal (a typical feature of APS pixels) into the CCD structure of Hasegawa wherein CCD and APS are obvious variations of each other as taught by Antonelli.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 7-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhou et al. (US Patent # 6,787,749).

[Claim 1]

Zhou et al. teach a photo-sensing array (figure 1, element 110) of a plurality of sensing pixels (210) arranged in rows and columns, each pixel having a photo-sensing element (211) to produce charge in response to incident photons from an object and an in-pixel circuit (213) to convert said charge into an electrical pixel signal representing said charge (col. 4 lines 61-67) and an integrator array (130) of a plurality of integrators (231) arranged in rows and columns respectively equal to said rows and columns of said photo-sensing array, wherein integrators of

each column are coupled to receive electrical pixel signals from only one designated column of sensing pixels in said photo-sensing array and are operable to produce time-delayed integration signals representing the object (col. 3 lines 44-51) after each sensing pixel is sampled and read out for a number of times equal to a number of said rows in said photo-sensing array (col. 8 lines 45-61).

[Claim 2]

Zhou et al. teaches a combination of capacitor (231) and transistor (232) is read as capacitor-switched integrator.

[Claim 7]

Zhou et al. teaches that the APS circuit having an amplifier (col. 1 lines 31-37).

[Claim 8]

Zhou et al. teaches that the APS circuit has a photo-gate (col. 4 lines 65-66).

[Claim 9]

Figure 3c discloses an equivalent reset circuit for all APS pixels (col. 6 lines 1-10).

[Claim 10]

Official Notice is taken of the fact that it is very well known in the art to have at least one ADC being used to digitize one output from an integrator array in order to edit the image digitally.

[Claim 11]

Zhou et al. teach that the APS pixel being consecutively sampled reset level and the signal level by the buffer 220 (col. 5 lines 8-13).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 16, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (US Patent # 5,917,620) in view of Antonelli et al. (US Patent # 6,259,108).

[Claim 16]

Hasegawa et al. teach a method comprising using a linear sensing array of pixels (col. 2 lines 65-67, figure 6, element 1701-1703). In a scanner it is very well known in the art that there is a relative direction of movement between the object and the sensors, coupling a linear integrator array (1710, 1712) of integrators sensing array to sample object generated by multiple frames sensing array (col. 3 lines 12-21) and images of the spatially shifting the mapping from the sensing frames along the predetermined direction to produce a summed signal that sums pixel signals from different pixel locations different frames corresponding common image from a location on object (col. 2 lines 56-64) except that each pixel internally converts radiation-induced charge into an electrical pixel signal. However Antonelli teaches a linear array sensor with a single linear array, or two or more parallel rows of light sensing pixels, may use CCD (charge coupled device) pixels, or may use CMOS (complementary metal oxide semiconductor) APS (active pixel sensing) pixels, photo-diode pixels, or any other linear array of light sensing technology (col. 4 lines 17-24). Therefore taking the combined teachings of Hasegawa and Antonelli, it would have been obvious to one skilled in the art at the time of the invention to have

been motivated to have an in-pixel circuit internally converting radiation-induced charge into an electrical pixel signal (a typical feature of APS pixels) into the CCD structure of Hasegawa wherein CCD and APS are obvious variations of each other as taught by Antonelli.

[Claim 17]

Official Notice is taken of the fact that it is notoriously common to sample twice the reset and signal levels (CDS) of a pixel during a frame in order to reduce noise.

[Claim 19]

See Claim 2.

Allowable Subject Matter

5. Claims 3-6, 12-15 and 18 are allowed.

See the previous office action for reasons of allowance.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
June 22, 2005

DAVID L. OMETZ
PRIMARY EXAMINER